

To: Facsimile Number: 703-872-9306

Total Pages Sent 9

From:

Texas Instruments Incorporated  
Facsimile: 972-917-4418

RECEIVED  
CENTRAL FAX CENTER

MAY 02 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant Vikas K. Agrawal, et al.

Docket Number: TI-35282

Serial No.: 10/663,575

Art Unit: 2824

Filed: 09/16/03

Examiner: Van Thu T. Nguyen

For: Cycle Ready Circuit for Self-Clocking Memory Device

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below:

Karen Vertz  
Karen Vertz

5-2-05  
Date

FACSIMILE COVER SHEET

<input checked="" type="checkbox"/> FACSIMILE COVER SHEET	<input checked="" type="checkbox"/> AMENDMENT <u>111 (8 pages)</u>
<input type="checkbox"/> NEW APPLICATION	<input type="checkbox"/> EOT
<input type="checkbox"/> DECLARATION	<input type="checkbox"/> NOTICE OF APPEAL
<input type="checkbox"/> ASSIGNMENT	<input type="checkbox"/> APPEAL <u>(# Pages)</u>
<input type="checkbox"/> FORMAL DRAWINGS	<input type="checkbox"/> ISSUE FEE & PUBLICATION FEE (1 Page)
<input type="checkbox"/> INFORMAL DRAWINGS	<input type="checkbox"/> REPLY BRIEF (IN TRIPLICATE) (# Pages)
<input type="checkbox"/> CONTINUATION APP'N	<input type="checkbox"/> ELECTION
<input type="checkbox"/> DIVISIONAL APP'N	
NAME OF INVENTOR(S): Vikas K. Agrawal, et al.	
RECEIPT DATE & SERIAL NO.: Serial No.: <b>10/663,575</b>	
TITLE OF INVENTION: Cycle Ready Circuit for Self-Clocking Memory Device Filing Date: 09/16/03	
TI FILE NO.: <b>TI-35282</b>	DEPOSIT ACCT. NO.: <b>20-0668</b>
FAXED: 5-2-05 DUE: 5-2-05 ATTY/SECY: AKS/kjv	

This facsimile is intended only for the use of the address named and contains legally privileged and/or confidential information. If you are not the intended recipient of this telecopy, you are hereby notified that any dissemination, distribution, copying or use of this communication is strictly prohibited. Applicable privileges are not waived by virtue of the document having been transmitted by Facsimile. Any misdirected facsimiles should be returned to the sender by mail at the address indicated on this cover sheet.

Texas Instruments Incorporated  
PO Box 655474, M/S 3989  
Dallas, TX 75285-5474

RECEIVED  
CENTRAL FAX CENTER

MAY 02 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Vikas K. Agrawal, et al. Art Unit: 2824  
Serial No.: 10/663,575 Examiner: Van Thu T. Nguyen  
Filed: 09/16/03 Docket: TI-35282  
For: CYCLE READY CIRCUIT FOR SELF-CLOCKING MEMORY DEVICE

Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

CERTIFICATION OF FACSIMILE TRANSMISSION  
I hereby certify that the above correspondence is  
being transmitted by facsimile to the U.S. Patent  
and Trademark Office at 703-872-9306 on the date  
shown below:

Karen Vertz  
Karen Vertz

5-2-05  
Date

AMENDMENT

In response to the Official Action in this case mailed  
February 2, 2005, please enter the following: